AMENDMENTS TO THE CLAIMS

1. (Currently Amended) An apparatus, comprising:

a buffer having a trigger, integrated on a component coupled with a simultaneous bi-directional (SBD) memory bus having ternary logic levels, the trigger is to facilitate un-intrusively observing, reading and echoing of one or more of a plurality of signals transmitted on the SBD memory bus, wherein the trigger operates to instruct the buffer using one or more of a control signal-based indication, an address signal-based indication, and a time-based indication; ~~and~~

a diagnostic device coupled with the buffer, the diagnostic device to facilitate one or more of detecting, accessing, and reading of the plurality of echoed signals;

an observability port coupled with the buffer, the observability port to receive the echoed signals, wherein the observability port comprises a logic observability port; and

an observability bus coupled with the observability port.

2-5. (Cancelled)

6. (Currently Amended) A method, comprising:

transmitting a plurality of signals on a simultaneous bi-directional (SBD) memory bus having ternary logic levels;

a buffer having a trigger, integrated on a component coupled with the bus, un-intrusively facilitating observing, reading and echoing of one or more of a plurality of signals transmitted on the bus, wherein the trigger operates to instruct the buffer using one or more of a control signal-based indication, an address signal-based indication, and a time-based indication; ~~and~~

a diagnostic device coupled with the buffer, the diagnostic device facilitating one or more of detecting, accessing, and reading of the plurality of echoed signals; and

an observability port coupled to the buffer and an observability bus, receiving the plurality of echoed signals, wherein the observability port comprises a logic observability port.

7-13. (Cancelled)

14. (Currently Amended) A system, comprising:

a memory;

an input/output (I/O) port;

a microprocessor;

a buffer, having a trigger, integrated on a component coupled with a simultaneous bi-directional (SBD) memory bus having ternary logic levels, the trigger is to facilitate un-intrusively observing, reading and echoing of a plurality of signals transmitted on the bus, wherein the trigger operates to instruct the buffer using one or more of a control signal-based indication, an address signal-based indication, and a time-based indication; ~~and~~

a diagnostic device coupled with the buffer, the diagnostic device to facilitate one or more of detecting, accessing, and reading of the plurality of echoed signals;

an observability port coupled with the buffer, the observability port to receive the echoed signals, wherein the observability port comprises a logic observability port; and

an observability bus coupled with the observability port.

15-22. (Cancelled)